What is Claimed is:

1. An integrated circuit device comprising:

a memory cell array that is configured to output a plurality of data bits in parallel at a first data rate; and

an output circuit that is configured to serially output the plurality of data bits to an external terminal at the first data rate in a normal mode of operation, and to serially output the plurality of data bits to the external terminal at a second data rate that is lower than the first data rate, in a test mode of operation.

2. An integrated circuit device according to Claim 1 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the first data rate is produced in response to both the rising edge and the falling edge of the clock signal and wherein the second data rate is produced in response to only one of the rising edge or the falling edge of the clock signal.

3. An integrated circuit device according to Claim 1 wherein the memory cell array is configured to output the plurality of data bits in parallel at the first data rate over a corresponding plurality of first data lines and wherein the output circuit is configured to serially output the plurality of data bits to the external terminal at the first data rate in the normal mode of operation using a corresponding plurality of second data lines, and to serially output the plurality of data bits to the external terminal at the second data rate that is lower than the first data rate using the corresponding plurality of second data lines in the test mode of operation.

4. An integrated circuit device according to Claim 1 wherein the output circuit is configured to replicate a first portion of the plurality of data bits that are output from the memory cell array in parallel to thereby serially output the first portion of the plurality of data bits to the external terminal at the second data rate that is lower than the first data rate, and to replicate a second portion of the plurality of data bits that are output from the memory cell array in parallel to thereby serially output the second portion of the plurality of data bits to the external terminal at the second data rate that is lower than the first data rate in the test mode of operation.

5. An integrated circuit device according to Claim 1 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the output circuit is responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal in the normal mode of operation, and is responsive to only one of the first internal clock signal or the second internal clock signal in the test mode of operation.

6. An integrated circuit device according to Claim 1 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the output circuit is responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal in the normal mode of operation, and is alternatingly responsive to the first internal clock signal and the second internal clock signal in the test mode of operation.

7. An integrated circuit device according to Claim 1 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the output circuit is responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal in the normal mode of operation, and is responsive to a divided first internal clock signal that is generated from the first internal clock signal and to a divided second internal clock signal that is generated from the second internal clock signal in the test mode of operation.

8. An integrated circuit device according to Claim 1:

wherein the memory cell array is configured to output the plurality of data bits in parallel at the first data rate over a corresponding plurality of first data lines; and

wherein the output circuit comprises a multiplexer that is configured to multiplex read data on the first data lines onto a corresponding plurality of second data lines, and an output buffer that is configured to serially output data on the second data lines to the external terminal.

9. An integrated circuit device according to Claim 8:

wherein the multiplexer is configured to couple a respective first data line to a respective second data line in the normal mode of operation, to couple respective even first data lines to respective even second data lines in a first submode of the test mode of operation, and to couple respective odd first data lines to respective odd second data lines in a second submode of the test mode of operation.

10. An integrated circuit device comprising::

a memory cell array that is configured to output a plurality of data bits in parallel at a first data rate over a corresponding plurality of first data lines;

an output circuit that is configured to serially output the plurality of data bits to an external terminal at the first data rate in a normal mode of operation, and to serially output the plurality of data bits to the external terminal at a second data rate that is lower than the first data rate, in a test mode of operation, the output circuit comprising a multiplexer that is configured to multiplex read data on the first data lines onto a corresponding plurality of second data lines, and an output buffer that is configured to serially output data on the second data lines to the external terminal;

a mode register set that is responsive to a plurality of command signals and is configured to generate first and second test mode signals to place the multiplexer in first and second submodes, respectively, of the test mode of operation;

wherein the multiplexer is configured to couple a respective first data line to a respective second data line in the normal mode of operation, to couple respective even first data lines to respective even second data lines in the first submode of the test mode of operation, and to couple respective odd first data lines to respective odd second data lines in the second submode of the test mode of operation, and comprises;

a first switch that is configured to couple a respective even first data line to a respective even second data line in the first submode;

a second switch that is configured to couple a respective odd first data line to a respective odd second data line in the second submode; and

an equalizing circuit that is configured to couple a respective odd second data line to a respective adjacent even second data line in the first and second submodes.

11. An integrated circuit device according to Claim 9 further comprising:

a mode register set that is responsive to a plurality of command signals and is configured to generate first and second test mode signals to place the multiplexer in the first and second submodes, respectively, of the test mode of operation.

12. An integrated circuit device, comprising:

a memory cell array that is configured to output a plurality of data bits in parallel at a first data rate over a corresponding plurality of first data lines;

an output circuit that is configured to serially output the plurality of data bits to an external terminal at the first data rate in a normal mode of operation, and to serially output the plurality of data bits to the external terminal at a second data rate that is lower than the first data rate, in a test mode of operation, the output circuit comprising a multiplexer that is configured to multiplex read data on the first data lines onto a corresponding plurality of second data lines, and an output buffer that is configured to serially output data on the second data lines to the external terminal;

a mode register set that is responsive to a plurality of command signals and is configured to generate first and second test mode signals to place the multiplexer in first and second submodes, respectively, of the test mode of operation;

wherein the multiplexer is configured to couple a respective first data line to a respective second data line in the normal mode of operation, to couple a respective first data line to a respective second data line in the first submode of the test mode of operation, and to cross-couple respective odd and even first data lines to respective even and odd second data lines in the second submode of the test mode of operation.

13. An integrated circuit device according to Claim 12 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the output buffer is responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal in the normal mode of operation, and is responsive to only one of the first internal clock signal and the second internal clock signal in the first and second submodes of the test mode of operation.

14. An integrated circuit device according to Claim 12 wherein the multiplexer comprises:

a first switch that is configured to couple a respective first data line to a respective second data line. in the first submode; and

a second switch that is configured to cross-couple respective odd and even first data lines to respective even and odd second data lines in the second submode.

15. An integrated circuit device according to Claim 13 wherein the output buffer comprises:

a corresponding plurality of registers, a respective one of which is configured to store read data from a respective first data line;

a latch that is associated with a respective pair of adjacent registers, a respective latch being configured to latch data from a first adjacent register in response to a first clock signal and to latch data from a second adjacent register in response to a second clock signal; and

a parallel-to-serial converter that is responsive to the latches, to the first and the second internal clock signals in the normal mode of operation, and to only one of the first and second internal clock signals during both the first and second submodes of operation.

16. An integrated circuit device according to Claim 1:

wherein the memory cell array is configured to output the plurality of data bits in parallel at the first data rate over a corresponding plurality of first data lines; and

wherein the output circuit comprises an output buffer that is configured to serially output data to the external terminal.

17. An integrated circuit device according to Claim 16 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the output buffer is responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal in the normal mode of operation, is responsive to only one of the first internal clock signal and the second internal clock signal in a first submode of the test mode of operation and is responsive to only the other of the first internal clock signal and the second internal clock signal in a second submode of the test mode of operation.

18. An integrated circuit device according to Claim 17 wherein the output buffer comprises:

a corresponding plurality of registers, a respective one of which is configured to store read data from a respective first data line;

a latch that is associated with a respective pair of adjacent registers, a respective latch being configured to latch data from a first adjacent register in response to a first clock signal and to latch data from a second adjacent register in response to a second clock signal; and

a parallel-to-serial converter that is responsive to the latches and to the first and second internal clock signals in the normal mode of operation, to only one of the first and second internal clock signals during the first submode of operation and to only the other of the first and second internal clock signals during the second submode of operation.

19. An integrated circuit device according to Claim 17 further comprising:

a mode register set that is responsive to a plurality of command signals and is configured to generate first and second test mode signals to place the output buffer in the first and second submodes, respectively, of the test mode of operation.

20. An integrated circuit device according to Claim 16 wherein the memory cell array is responsive to a clock signal having rising and falling edges, wherein the output buffer is responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal in the normal mode of operation, and is responsive to a divided first internal clock signal and a divided second internal clock signal in the test mode of operation.

21. An integrated circuit device according to Claim 20 wherein the divided first internal clock signal and the divided second internal clock signal are respectively of half the frequency of the first internal clock signal and the second internal clock signal.

22. An integrated circuit device according to Claim 20 further comprising:

a mode register set that is responsive to a plurality of command signals and is configured to generate a test mode signal to place the output buffer in the test mode of operation.

23. An integrated circuit device according to Claim 20 further comprising:

a first dividing circuit that is configured to generate the divided first internal clock signal in response to the rising edge of the clock signal and a test mode select signal; and

a second dividing circuit that is configured to generate the divided second internal clock signal in response to the falling edge of the clock signal and the test mode select signal.

24. An integrated circuit device according to Claim 23:

wherein the first dividing circuit comprises a first divider that is responsive to the rising edge of the clock signal and the test mode signal; and

wherein the second dividing circuit comprises a second divider that is responsive to the falling edge of the clock signal and the test mode signal, and a delay element that is responsive to the second divider.

25. A method of operating an integrated circuit device having a memory cell array that is configured to output a plurality of data bits in parallel at a first data rate, the method comprising:

serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation; and

serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation.

26. A method according to Claim 25:

wherein serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation comprises serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation, in response to rising and falling edges of a clock signal; and

wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation comprises serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation, in response to only one of the rising edge or the falling edge of the clock signal.

27. A method according to Claim 25 wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation comprises:

replicating a first portion of the plurality of data bits that are output from the memory cell array in parallel to thereby serially output the first portion of the plurality of data bits to the external terminal at the second data rate that is lower than the first data rate; and

replicating a second portion of the plurality of data bits that are output from the memory cell array in parallel to thereby serially output the second portion of the plurality of data bits to the external terminal at the second data rate that is lower than the first data rate.

28. A method according to Claim 25:

wherein the memory cell array is responsive to a clock signal having rising and falling edges;

wherein serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation comprises serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal; and

wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation comprises serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate responsive to only one of the first internal clock signal and the second internal clock signal.

29. A method according to Claim 25:

wherein the memory cell array is responsive to a clock signal having rising and falling edges;

wherein serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation comprises serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal; and

wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation comprises serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate responsive alternatingly to the first internal clock signal and the second internal clock signal.

30. A method according to Claim 25:

wherein the memory cell array is responsive to a clock signal having rising and falling edges;

wherein serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation comprises serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate responsive to a first internal clock signal that is generated in response to the rising edge of the clock signal and to a second internal clock signal that is generated in response to the falling edge of the clock signal; and

wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate, in a test mode of operation comprises serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate responsive to a divided first internal clock signal that is generated from the first internal clock signal and to a divided second internal clock signal that is generated from the second internal clock signal.

31. A method according to Claim 25:

wherein the memory cell array is configured to output the plurality of data bits in parallel at the first data rate over a corresponding plurality of first data lines and the memory device is configured to output the plurality of bits in to an output terminal over a corresponding plurality of second data lines;

wherein serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation comprises coupling a respective first data line to a respective second data line in the normal mode of operation; and

wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation comprises coupling respective even first data lines to respective even second data lines in a first submode of the test mode of operation, and coupling respective odd first data lines to respective odd second data lines in a second submode of the test mode of operation.

32. A method according to Claim 25:

wherein the memory cell array is configured to output the plurality of data bits in parallel at the first data rate over a corresponding plurality of first data lines and the memory device is configured to output the plurality of bits in to an output terminal over a corresponding plurality of second data lines;

wherein serially outputting the plurality of data bits from the memory cell array to an external terminal at the first data rate in a normal mode of operation comprises coupling a respective first data line to a respective second data line in the normal mode of operation; and

wherein serially outputting the plurality of data bits from the memory cell array to the external terminal at a second data rate that is lower than the first data rate in a test mode of operation comprises coupling a respective first data line to a respective second data line in a first submode of the test mode of operation and cross coupling respective odd and even first data lines to respective even and odd second data lines in a second submode of the test mode of operation.